DESIGNING WITH OFF-THE-SHELF LINEAR MICROCIRCUITS*

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I. INTRODUCTION

Without a doubt, the most significant advantage of monolithic integrated circuits is low cost. This means not only lower initial parts cost but also reduced expense in assembly and testing. However, in order to realize this, it is necessary that the microcircuit be manufactured in large volume with consistently high yields.

To achieve large-volume production, some sort of standardization is required. This is a particular problem with linear microcircuits since there is a much wider range of analog functions which generally have individual usage less than equivalent digital circuits. However, the advantages of well-accepted standard circuits are many. For the user, it boils down to immediate availability of a completely specified product at low cost.

This paper will discuss the use of off-the-shelf linear microcircuits in circuit design. It does not advocate totally integrating a system. Instead, it is recommended that integrated circuits be used where possible, but with discrete components added to provide flexibility or to accomplish functions which are not economically integrated. This approach is based on the fact that well-designed integrated circuits are not too much more difficult to make than individual transistors. Therefore, a relatively simple discrete component amplifier can, for example, be replaced with an integrated operational amplifier realizing an advantage in both price and performance—even though this approach would be absurd with discrete parts. This optimum usage of discrete parts and standard integrated circuits for maximum cost effectiveness should present a much greater challenge to the design engineer than might have been taken away by the advent of integrated circuits.

The integrated circuits to be discussed here are the μA702A wideband DC amplifier,[1,2,3,4] the μA709 high-performance operational amplifier,[5] the μA710 high-speed differential comparator,[6] and the μA711 dual comparator.[6,7] Detailed information on their design, operation, and characteristics will not be given here but is adequately covered in the references, as are additional applications. A brief summary of the performance of these devices is given in Table I.

II. SINE WAVE OSCILLATOR

The first circuit to be discussed is a phase-shift oscillator using the μA702A wideband DC amplifier. The schematic is shown in Fig. 1. Negative feedback is applied to the inverting input of the amplifier through R_3 to stabilize the gain and make it essentially independent of the integrated circuit characteristics. The R-C network (R_1, C_1, R_2, and C_2) applies positive feedback to the noninverting input. The circuit will oscillate at the frequency where the phase shift through the R-C network is zero, as long as the positive feedback is equal to or greater than the negative feedback. It is desirable to maintain the positive feedback exactly equal to the negative feedback: if the positive feedback is greater, the output of the oscillator will build up until it becomes nonlinear, thereby distorting the output sine wave. The positive and negative feedback cannot be made equal with a simple adjustment since any small component change will either cause the circuit to stop oscillating or distort. This difficulty is overcome using an AGC circuit which holds the gain at the precise value required to sustain oscillation at the desired output level.

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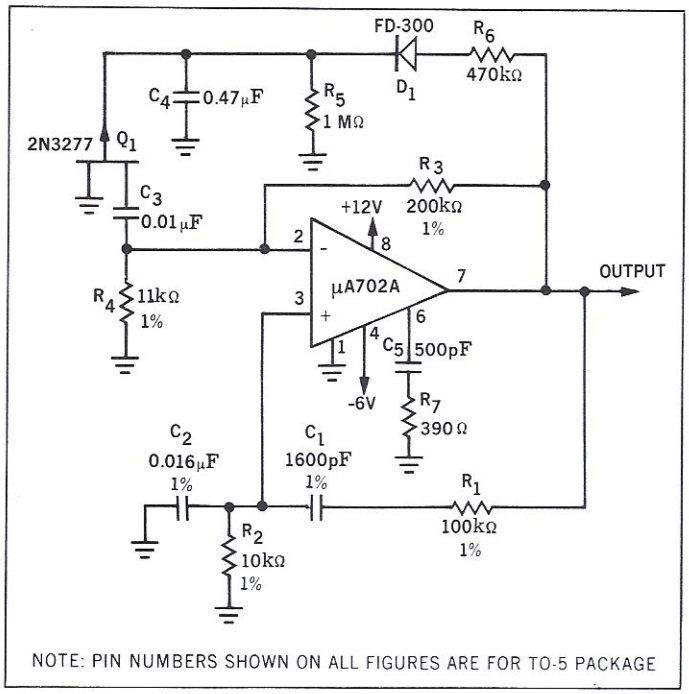

Fig. 1. 1 kHz sine-wave oscillator.

If $R_1 C_1 = R_2 C_2$, the frequency where the phase shift through the R-C network is zero (and therefore the frequency of oscillation) is given by

$$f = \frac{1}{2\pi R_1 C_1} \qquad (1)$$

The attenuation through the network at this frequency is

$$\eta = \frac{1}{1 + 2\frac{R_1}{R_2}} \qquad (2)$$

The amplifier gain must make up for this loss for oscillation to be possible. For $R_1 = 10 R_2$ the amplifier gain must be exactly 21. A large ratio of R_1 to R_2 is chosen to keep the signal level across the gain-regulating FET low enough to avoid distortion.

The output of the amplifier is rectified by D_1 and filtered by C_4. This voltage, which varies as the AC output of the amplifier, is fed to the gate of the FET. The drain-to-source resistance of the FET is controlled by this voltage to hold the output of the amplifier at a constant level. The filter capacitor, C_4, must be large enough for stability of the AGC loop. The value of C_3 is also important for AGC stability. To change the frequency of oscillation, C_1, C_2, C_3, and C_4 should all be changed in proportion. The AC output level is determined by the ratio R_6/R_5 and the characteristics of the FET.

With the component values shown, the frequency of oscillation is 1 kHz and the peak-to-peak output voltage is about 8 V. The stabilization time from initial turn-on is approximately 50 ms.

III. VOLTAGE-TO-FREQUENCY CONVERTER

An excellent example of the design philosophy being presented in this article is the voltage-to-frequency converter shown in Fig. 2. The circuit consists of an integrator, a voltage comparator and switch. The output voltage of the

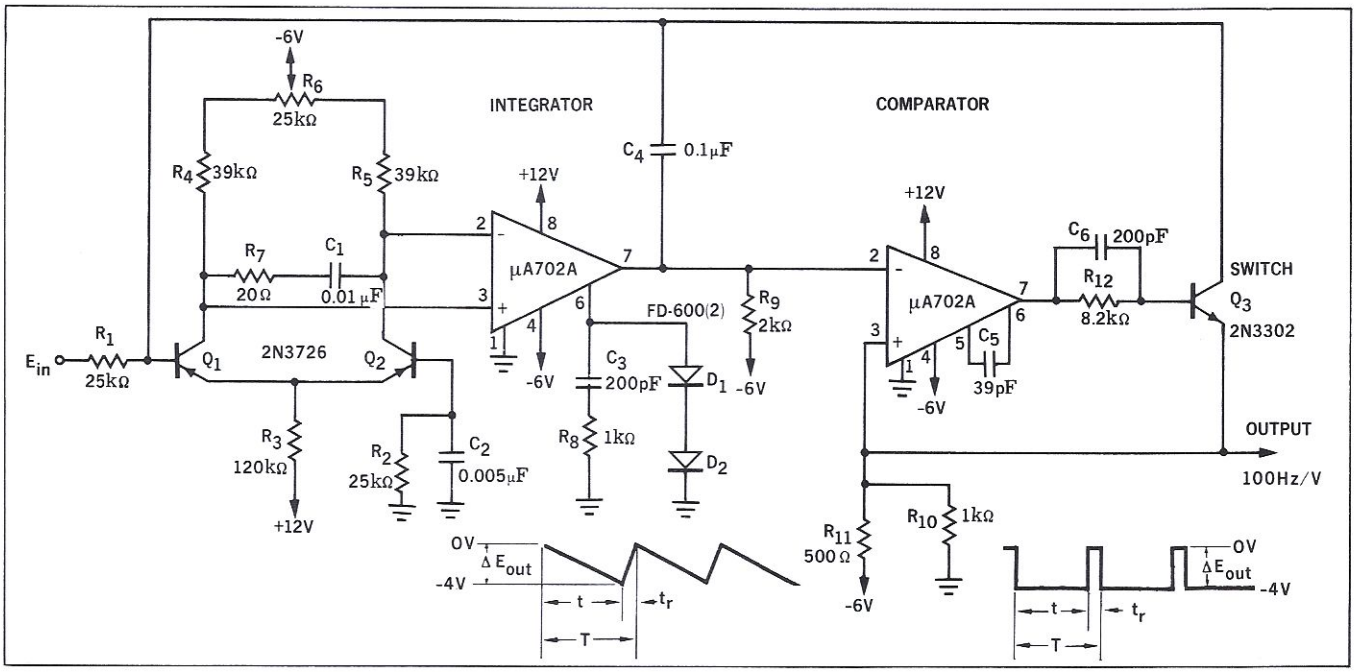

Fig. 2. Voltage-to-frequency converter.

integrator is a negative-going ramp which falls at a rate that is directly proportional to the DC input signal. When the output of the integrator reaches a predetermined negative level, it is sensed by the comparator which drives the switch to reset the integrator output to zero; the cycle is then repeated. The time required for the integrator output to go from zero to the preset level is inversely proportional to the input voltage so the operating frequency will be proportional to this voltage.

The μA 702A is chosen for the integrator because of the fast slewing rate required during the reset interval. However, the μA 702A alone does not have enough gain to make the integrator function properly over a wide dynamic range. In addition, lower input currents than are practical with the μA 702A are frequently required in this application. Both these limitations are overcome by using a discrete PNP matched pair (Q_1 and Q_2) in front of the amplifier. This composite amplifier has a gain greater than 25,000 and input currents less than 0.5 μA. The offset voltage of the input transistors is conveniently balanced out with the potentiometer (R_6) shown in the schematic. Because of the high gain of the complete amplifier, frequency compensation is done at two points with R_7 - C_1 and R_8 - C_3 as shown in the figure. The integrating capacitor is C_4. The clamping diodes (D_1 and D_2) prevent overloading of the comparator under abnormal operating conditions.

A second μA 702A is used as a voltage comparator at the output of the integrator. A threshold voltage of -4.0 V is supplied to the noninverting input of the comparator from a resistive divider (R_{10} and R_{11}). When the output of the integrator falls to -4.0 V, the output of the comparator rises rapidly from -5.0 V, turning on Q_3 which supplies positive feedback to the noninverting input of the comparator. Q_3 saturates and drives approximately 11 mA into the summing node of the integrator; it also holds the noninverting input of the comparator very near to ground potential. When the integrator output, which is being driven positive by the switch current, reaches zero, the comparator output swings negative and turns off Q_3. The cycle is then repeated. In Fig. 2, R_{12} limits the base drive of Q_3 while C_5 and C_6 decrease the turn-on and turn-off times of the switch.

The time required for a given change in the output voltage of the integrator is given in terms of the input voltage and circuit values by

$$t = R_1 C_4 \frac{\Delta E_{OUT}}{E_{IN}} \tag{3}$$

Similarly, when Q_3 is turned on, the reset time is

$$t_r = C_4 \frac{\Delta E_{OUT}}{I_{C3}} \tag{4}$$

or

$$t_r \cong R_{11} C_4 \frac{\Delta E_{OUT}}{V^-} \tag{5}$$

The output of the integrator swings from zero to a voltage determined by the resistive divider, R_{10} and R_{11}, so

$$\Delta E_{OUT} = \frac{R_{10} V^-}{R_{10} + R_{11}} \tag{6}$$

Therefore, the period for one cycle of operation is

$$T = \frac{C_4 R_{10} V^-}{R_{10} + R_{11}} \left(\frac{R_1}{E_{IN}} + \frac{R_{11}}{V^-} \right) \tag{7}$$

Since $\frac{R_1}{E_{IN}} >> \frac{R_{11}}{V^-}$, we can write

$$f \cong \frac{(R_{10} + R_{11}) E_{IN}}{C_4 R_1 R_{10} V^-} \tag{8}$$

This gives a conversion factor of 100 Hz/V.

IV. LOGARITHMIC AMPLIFIER

The bipolar transistor is probably the most predictable nonlinear element known to physics. It is established in Ref. 8 that the variation in collector current with emitter-base voltage is given by

$$I_C \propto \exp\left(\frac{q V_{BE}}{kT}\right) \tag{9}$$

where $V_{BE} > \frac{4kT}{q}$.

In this equation, q is the charge of an electron, k is Boltzmann's constant and T is the absolute temperature. The expression holds up to high currents where emitter contact and base spreading resistances become important and down to low currents where collector leakages cause inaccuracy.

The expression is valid for operation over at least six decades of collector current with well-made silicon transistors. This contrasts with similar expressions for diode current and the emitter current of transistors which show substantial error over three decades of current operation.

Using the expression given above, it can be shown [9] that the emitter-base voltage differential between two matched transistors operating at different collector currents is

$$\Delta V_{BE} = \frac{kT}{q} \ln\left(\frac{I_{C1}}{I_{C2}}\right) \tag{10}$$

In the circuit of Fig. 3, a transistor (Q_1) is used as the feedback element around a μA 709 operational amplifier. The negative feedback forces the collector current of Q_1 to be equal to the current into the summing node of the amplifier. Hence, we can write

$$I_{C1} = \frac{E_{IN}}{R_1} \tag{11}$$

The collector current of Q_2 is determined by the positive supply voltage and R_6 as

$$I_{C2} = \frac{V^+}{R_6} \tag{12}$$

If Q_1 and Q_2 are a matched pair of transistors, Eq. (10) can be used to give

$$\Delta V_{BE} = \frac{kT}{q} \ln\left(\frac{R_6 E_{IN}}{R_1 V^+}\right) \tag{13}$$

Since the base of Q_1 is grounded, the negative of this voltage is presented to the input of the second amplifier. The gain of this stage is

$$A_V = \frac{R_7 + R_8}{R_7}$$

so

$$E_{OUT} = -\frac{kT(R_7 + R_8)}{qR_7} \ln\left(\frac{R_6 E_{IN}}{R_1 V^+}\right) \tag{14}$$

which shows that the output voltage is proportional to the logarithm of the input voltage. It can be seen from Eq. (14) that the coefficient of the log term is proportional to absolute temperature, which gives it a thermal sensitivity of 0.3%/°C. The over-all transfer function of the amplifier is given for various operating temperatures in Fig. 3. As shown, the amplifier has an 80-dB dynamic range.

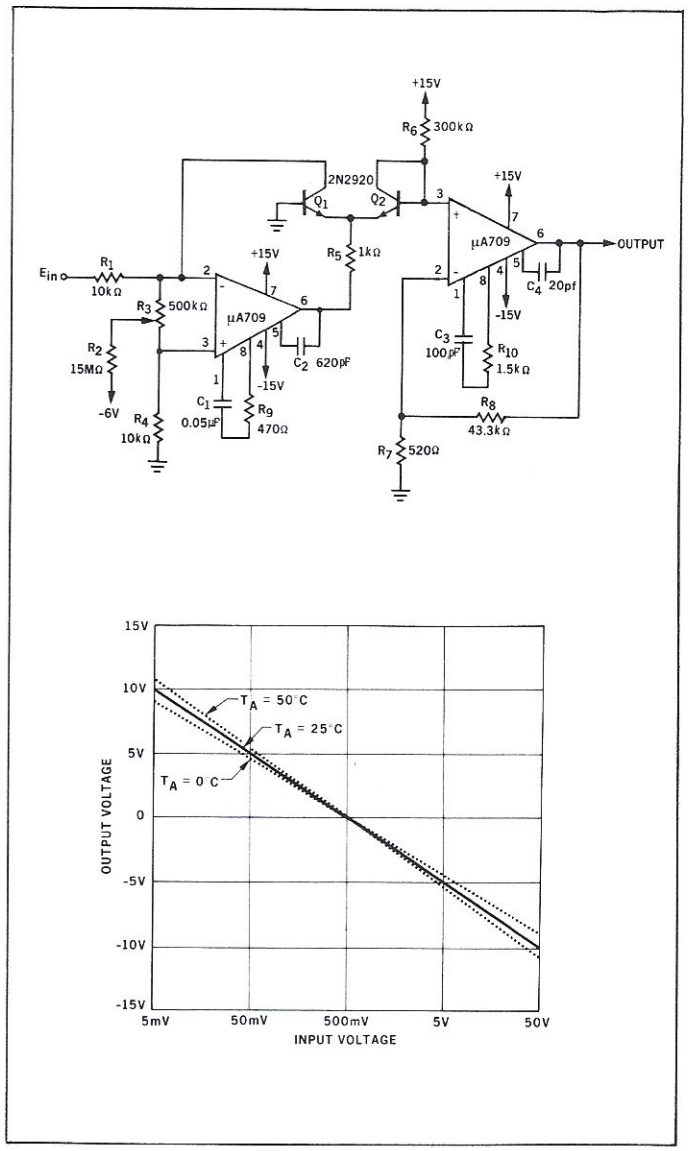

Fig. 3. Logarithmic amplifier.

Additional details of the circuit in Fig. 3 are that R_2 and R_3 are used to provide an offset adjustment, which increases the dynamic range for small input signals. R_5 is used to limit the loop gain of the input amplifier so that it can be frequency compensated. R_7 is chosen to be equal to the diode impedance of Q_2 to minimize the effect of the input bias current of the output amplifier. The slope of the log characteristic is determined by R_8 while R_6 determines the zero crossing.

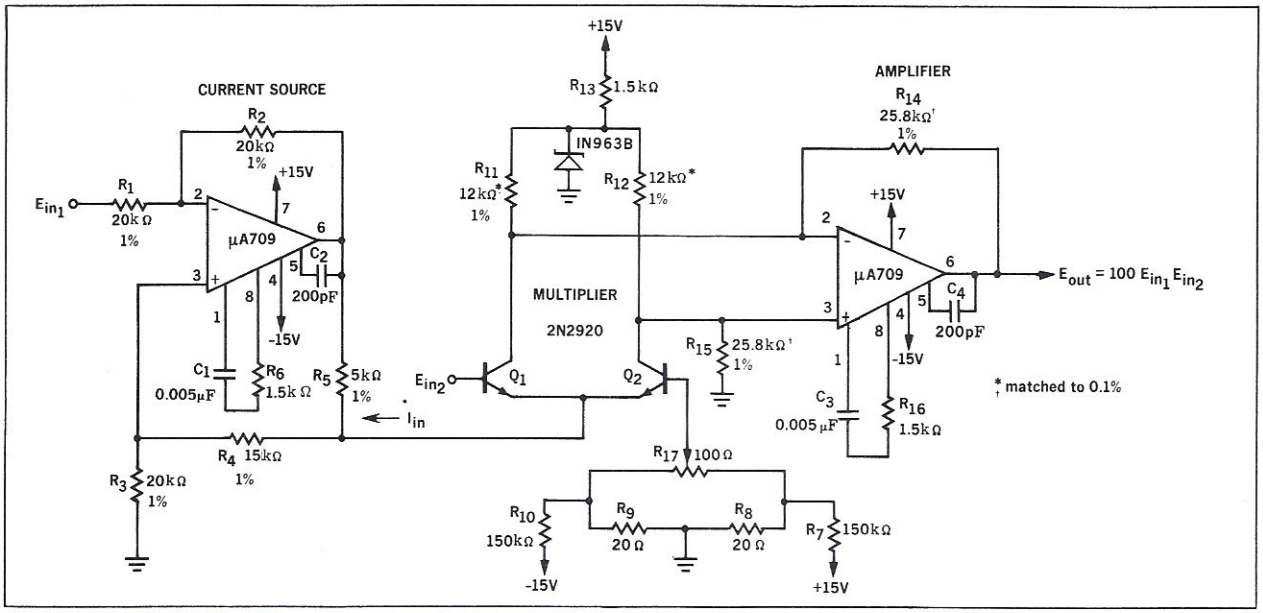

Fig. 4. Multiplier.

V. MULTIPLIER

Another interesting use for the nonlinear properties of the bipolar transistor is the multiplier shown in Fig. 4. The basic multiplying element is the transistor pair, Q_1 and Q_2. Its operation can be understood from the following:

The small signal transconductance of a transistor can be obtained by differentiation of Eq. (9):

$$\frac{dI_C}{dV_{BE}} = \frac{qI_C}{kT} \tag{15}$$

A matched transistor pair in a differential configuration as shown in Fig. 4 will now be considered. For zero differential input voltage, the input current supplied to the emitters will split equally between the two transistors and the differential output current will be zero. Hence, Eq. (15) can be rewritten in terms of the differential output current, the input current to the emitters, and the input voltage as

$$I_{OUT} = \frac{q}{2kT} I_{IN} E_{IN\,2} \tag{16}$$

Hence, the differential output current is proportional to the product of the differential input voltage and the current supplied to the emitters.

In Fig. 4, the first μA 709 supplies a current that is proportional to a positive input voltage to the emitters of Q_1 and Q_2. Using standard operational amplifier theory, this current can be shown to be

$$I_{IN} = \frac{E_{IN\,1} R_2}{R_5 R_1} \tag{17}$$

A second input voltage is supplied to the differential pair. Combining Eqs. (16) and (17) and setting $R_1 = R_2$, the output current of the differential pair is

$$I_{OUT} = \frac{q}{2kTR_5} E_{IN\,1} E_{IN\,2} \tag{18}$$

The output of the pair is connected to a second μA 709 that converts the differential current to a single-ended, zero-referred voltage. The output voltage of this amplifier will be $E_{OUT} = R_{14} I_{OUT}$, for $R_{14} = R_{15}$ and $R_{11} = R_{12}$. Hence,

$$E_{OUT} = \frac{qR_{14}}{2kTR_5} E_{IN\,1} E_{IN\,2} \tag{19}$$

which shows that the output voltage is proportional to the product of the two input voltages.

There are several hints that are pertinent to making the circuit work right. One is that the resistor pairs R_{11} - R_{12} and R_{14} - R_{15} must be very closely matched (within 0.1 percent). An adjustment is provided for nulling the offset of Q_1

and Q_2. This adjustment should be made when the current-source current is at its maximum value. It should also be noted that Eq. (16) is a small-signal approximation, so the voltage input to the differential pair should be kept small. Restricting the input voltage to ± 20 mV gives linearity that is acceptable for the majority of applications. It should also be pointed out that $E_{IN\,2}$ can be a bipolar signal while $E_{IN\,1}$ must be a positive voltage.

VI. SERVO CURRENT DRIVER

A fairly typical example of an application where an operational amplifier would normally not be considered but a μA 702A can be used quite effectively is shown in Fig. 5. This is a push-pull, Class-B, servo current driver.

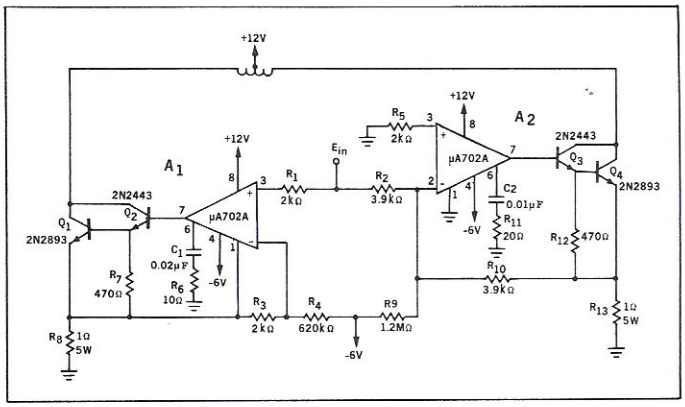

Fig. 5. Class-B servo current driver.

The output current of opposite sides is sensed across R_8 and R_{13}. One μA 702A (A_1) functions as a unity-gain, non-inverting amplifier that makes the voltage across R_8 equal to the input voltage for positive input signals. For negative input signals, A_2 functions as a unity-gain, inverting amplifier that forces the voltage across R_{13} to be equal to the input voltage. Thus, phase inversion for the push-pull amplifier is obtained. The quiescent output current of the amplifier is determined by R_4 and R_9. The values shown give a quiescent current of approximately 20 mA on each side. The circuit will give a ± 2 A output current for a ± 2 V input signal. The input resistance is 4 kΩ.

It is immediately obvious that the excellent DC characteristics of the μA 702A permit biasing of the output stage at very low quiescent currents without running the risk of thermal runaway or of encountering a dead zone — even for operation over the full temperature range. It is also apparent that the low offset and high gain allow good accuracy without wasting an excessive amount of the supply voltage across the current-sensing resistors. Since the output transistors are included within the feedback loop, their characteristics have a negligible effect on over-all performance.

One unusual aspect of this circuit is that the ground terminal of A_1 (pin 1) is connected to the current-sensing resistor, R_8. This provides bootstrapping on the common mode range of the amplifier so that it can be operated above its usual common mode limit of + 0.5 V without exceeding ratings.

VII. VOLTAGE COMPARATOR

Basically a voltage comparator does the same job as an operational amplifier. In fact, operational amplifiers are frequently used as comparators. However, in many applications the comparator is expected to recover rapidly from saturation, which is its normal operating state. Additionally, the large output swing desired for operational amplifiers is often a disadvantage when the comparator is used to drive low-level logic circuits. The μA 710 is a differential comparator that is designed to overcome the limitations of operational amplifiers in these applications. It features extremely fast recovery from saturation and the output is compatible with practically all integrated logic forms.

One of the most obvious applications for this device is as the voltage comparator in an A/D converter. For very high-speed systems in which the ladder network has a low impedance, the μA 710 can be used alone. However, when speed is not the prime objective the ladder impedance is generally high enough that the μA 710 introduces significant error due to loading. In this case, a transistor pair can be used in front of the μA 710 to reduce the input current. This is shown in Fig. 6. A PNP pair is used here so that the full ± 5 V input voltage range will still be available.

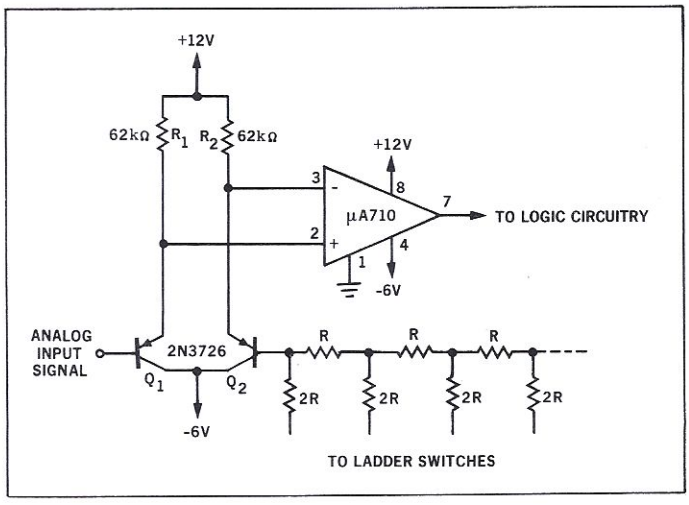

Fig. 6. Voltage comparator with optional input buffer for high input impedance.

The speed of the comparator is affected somewhat by the addition of the input stage. This is caused primarily by collector-base capacitance of the input transistor loading the ladder network. The transistors selected for this application have a low collector-base capacitance and should load the ladder with a total capacitance less than 10 pF.

VIII. POSITIVE PEAK DETECTOR

One difficult problem that can be solved with the μA710 is the accurate measurement of the peak amplitude of very fast pulses. A peak detector which does this is shown in Fig. 7. The input signal is applied to the noninverting input of the μA710. The output is taken from a large capacitor connected to the inverting input. If the voltage on the input terminal is greater than that on the output, the comparator output will swing positive and charge the capacitor rapidly through D_1. When the input voltage drops below the voltage on the capacitor, the output of the μA710 swings negative and the diode becomes reverse-biased. This leaves the capacitor charged to the peak value of the input signal.

Because of the low offset and fast response time of the μA710, the circuit can measure the amplitude of pulses less than 100 ns wide with an accuracy of 5 mV. The operating range of the circuit, which is determined by the available output swing of the comparator, is 0 to +2.5 V. The decay time of the voltage developed across the capacitor is determined by the input bias current of the μA710. This is approximately 20 ms/V. If it is desired that the peak detector follow more rapidly varying signals, a resistor can be inserted between the output and the negative supply voltage. The peak detector loads the signal source very little. The maximum current drawn from the source is approximately 25 μA, and this only occurs at the peak of the input signal.

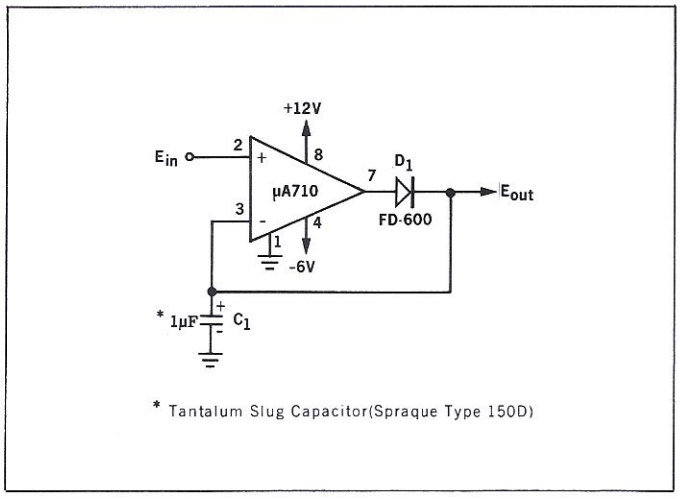

Fig. 7. Positive peak detector for fast pulses.

The circuit functions as a unity-gain feedback amplifier at the peak of the input signal with C_1 providing frequency compensation. Hence, C_1 cannot be made much smaller than the 1 μF indicated or the circuit will oscillate at the peak of the input signal, giving erratic operation. However, larger values of capacitance can be used.

IX. DOUBLED-ENDED LIMIT DETECTOR

The μA711 dual comparator was designed primarily for core-memory sense amplifier applications. However, it is sufficiently versatile to be used in a number of other applications. One of these is shown in Fig. 8. The circuit gives a positive output for input signals below a preset threshold or above a second, independently adjustable voltage threshold. This output is fed to a lamp driver; hence, whenever the input signal goes outside the tolerance limits, the lamp will light. A feature of the circuit is that the limit detector can be disabled when it is not being used by applying a zero logic signal to the strobe terminals. In addition, up to eight dual comparators can be wired with common outputs and be used to feed a single lamp driver.

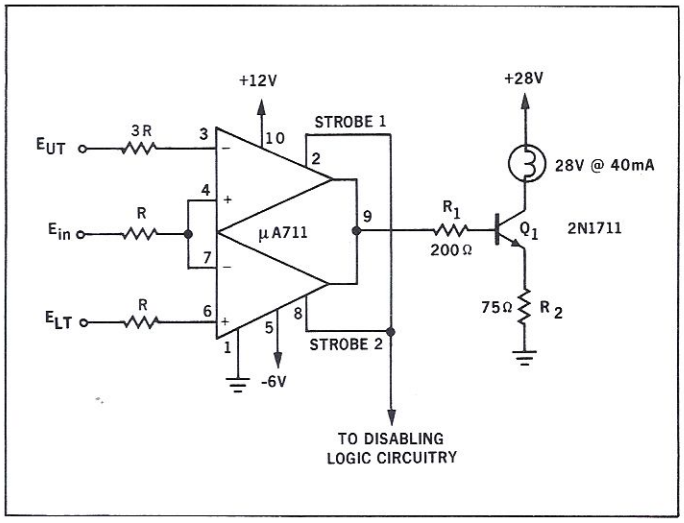

Fig. 8. Double-ended limit detector for automatic go/no-go test equipment.

Details of the design are that the relative values of the source resistances for the signal and reference voltages should be as indicated in the schematic to make the accuracy dependent only on offset currents rather than bias currents. Ideally, these resistances should be as low as possible. The lamp driver design is such that its peak output current is limited during the initial turn-on of the bulb when the filament resistance is low. This is accomplished with R_2. Series resistor R_1 limits the output current of the comparator when the lamp driver saturates.

X. CONCLUSION

The use of standard linear integrated circuits in a number of practical circuit designs has been described. Outstanding characteristics of integrated circuits have been used to eliminate parts that normally would be used but cannot be easily integrated. An example of this is the use of DC amplifiers that can be easily integrated instead of AC coupled amplifiers, thereby eliminating large capacitors. The majority of the circuitry has been integrated in these designs, but a number of discrete parts have been used. Leaving these components outside the described devices has made them versatile enough to be used in a large number of applications. In addition, many of these discrete parts (i.e., precision or large-value resistors as well as high-voltage, high-current or decent PNP transistors) would at best be very expensive to integrate. This approach not only results in a low-cost design by taking advantage of the best features of monolithic construction but also makes use of integrated circuits that can be manufactured easily and for which delivery is assured.

All the integrated circuits used here are available as off-the-shelf items from Fairchild Semiconductor distributors.

XI. REFERENCES

1. R. J. Widlar, "A Monolithic Operational Amplifier," Fairchild Semiconductor APP-105/2.

2. R. J. Widlar, "The Improved μA702 Wideband DC Amplifier," Fairchild Semiconductor APP-111/2.

3. "μA702 Circuit Design Ideas," Fairchild Semiconductor App-114.

4. J. N. Giles, "Frequency Compensation Techniques for an Integrated Operational Amplifier," Fairchild Semiconductor APP-117.

5. R.J. Widlar, "A Unique Circuit Design for a High Performance Operational Amplifier Especially Suited to Monolithic Construction," Fairchild Semiconductor TP-32.

6. R.J. Widlar, "The Operation and Use of a Fast Integrated Circuit Comparator, "Fairchild Semiconductor APP-116.

7. R. J. Widlar, "Core Memory Sense Amplifier Designs Using an Integrated Dual Comparator," Fairchild Semiconductor APP-123.

8. C. T. Sah, "Effect of Surface Recombination and Channel on P-N Junction and Transistor Characteristics," IRE Trans. on Electron Devices, Vol. ED-9, pp. 94-108, January 1962.

9. R.J. Widlar, "Some Circuit Design Techniques for Linear Integrated Circuits, "Fairchild Semiconductor TP-33.

TABLE I

TYPICAL CHARACTERISTICS OF THE DEVICES USED IN THE TEXT

Characteristic	μA702A	μA709	μA710	μA711
Input Offset Voltage	2 mV	1 mV	1 mV	1 mV
Input Offset Current	0.5 μA	50 nA	0.5 μA	0.5 μA
Input Bias Current	4 μA	200 nA	25 μA	25 μA
Temperature Coefficient of Input Offset Voltage	5 μV/°C	3 μV/°C	3 μV/°C	3 μV/°C
Input Voltage Range	+0.5, -4.0 V	±10 V	±5 V	±5 V
Common Mode Rejection	90 dB	90 dB	90 dB	90 dB
Voltage Gain	2700	45, 000	1500	1500
Output Voltage Swing	±5 V	±13 V @ 5 mA	+3.2, -0.5 V	+4.5, -0.5 V
Output Resistance	200 Ω	150 Ω	150 Ω	200 Ω
Power Consumption	70 mW	80 mW	110 mW	130 mW
Bandwidth	30 MHz	0.5 MHz	- -	- -
Response Time	- -		40 ns	40 ns
Strobe Release Time	- -	- -	- -	12 ns